



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yang, *et al.*

Attorney Docket: TSM03-0589

Filed: December 1, 2003

Examiner: TBD

Serial No.: 10/725,234

Art Unit: 2811

For: Multilayered Dual Bit Memory Device with Improved Write/Erase Characteristics and Method of Manufacturing

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & B that may be considered material to the examination of the above-identified application.

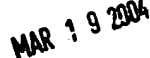
No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

15 March 04
Date

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/725,234
Filing Date	December 1, 2003
First Named Inventor	Yang, <i>et al.</i>
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	TSM03-0589

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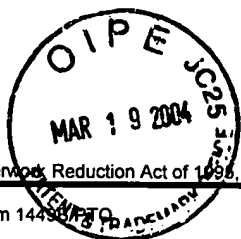
[illegible][illegible]

Date
Considered

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Sheet 2 of 2

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Examiner Name	Unknown
Attorney Docket Number	TSM03-0589

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		HSU, John Y., "Flash Memory Design," [online] http://www.ewh.ieee.org/r6/central_coast/Hsu2001.html (December 4, 2001) pp. 1-8.	
		LAMMERS, D., "AMD Pits MirrorBit Against Intel StrataFlash," [online] http://www.eetimes.com/story/OEG20020513S0012 (May 13, 2002) pp. 1-2.	
		EITAN, B., et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," IEEE Electron Device Letters, Vol. 21, No. 11 (November 2000) pp. 543-545.	
		LUSKY, E., et al., "Electrons Retention Model for Localized Charge in Oxide-Nitride-Oxide (ONO) Dielectric," IEEE Electron Device Letters, Vol. 23, No. 9 (September 2002) pp. 556-558.	
		"ETOX Flash Memory Technology: Scaling and Integration Challenges" Intel Technology Journal, Vol. 6, Issue 2 (May 16, 2002) pp. 27-30.	

Examiner Signature	Date Considered
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